FS8308 Low Power PLL Frequency Synthesizer IC

Advance Information

Description

The FS8308 is a serial data input, phase-locked loop IC with programmable input and reference frequency dividers. When combined with a VCO, this IC becomes the core of a very low power frequency synthesizer well-suited for mobile communication applications, e.x. paging systems and family radio service (FRS). There are some features implemented in this IC, including an 18-bit programmable input frequency divider, a terminal for reference oscillator buffer output, as well as stand-by control through programming, and etc. Details are listed in the following.

Features

- Up to 40 MHz external crystal oscillator reference frequency under normal condition
- Low current consumption ($I_{DD,total}$ typically 1.2 mA at f_{FIN} = 500 MHz and V_{DD1} = 1.0 V)
- With Schmitt trigger added for noise-immune programming input
- 18-bit programmable input frequency divider (including a ÷ 64/65 prescaler) with divide ratio range from 4032 to 262143
- 13-bit programmable reference frequency divider (including a ÷ 8 prescaler) with divide ratio range from 40 to 65528
- Optional lock detector output (*LD*, $f_R/2$, $f_V/2$)
- Charge pump output for passive low-pass filter
- Wide tuning range of charge pump output for external VCO (V_{SS}+*0.5 to* V_{DD2}-*0.5*)
- Switchover terminal for constant of loop filter or general open drain output
- Reference oscillator buffer output
- Programmable stand-by control
- TSSOP 16L package (0.65mm pitch)

Applications

- Pager
- Family radio service (FRS)
- Wireless communication system